IN THE CLAIMS

Please cancel claims 8, 19, and 21 without prejudice. Claims 1, 7, 11-14 and 18 have been amended. Claims 24-31 are new.

1. (Currently Amended) A method comprising:

disposing a trench layer upon a semiconductor substrate;

~~selectively removing a portion of the trench layer such that a remainder of the trench layer forms one or more trenches, the removal of a portion of the trench layer~~ forming one or more trenches in the trench layer exposing the semiconductor substrate;

filling the one or more trenches with a semiconductor material contacting the semiconductor substrate; and

~~removing any excess semiconductor material from the one or more trenches; and~~

removing ~~an additional~~[[a]] portion of the trench layer to expose the semiconductor material as one or more semiconductor fins.

2. (Original) The method of claim 1 wherein the trench layer is comprised of a plurality of layers.

3. (Original) The method of claim 2 wherein the plurality of layers include a first oxide layer disposed upon the semiconductor substrate, a nitride layer disposed upon the first oxide layer, and a second oxide layer disposed upon the nitride layer.

4. (Original) The method of claim 3 wherein removing an additional portion of the trench layer comprises removing any remaining portion of the second oxide layer, any remaining portion of the nitride layer, and retaining at least some portion of any remaining portion of the first oxide layer.

5. (Original) The method of claim 1 wherein the one or more trenches have a depth of approximately 10 nm.

6. (Original) The method of claim 5 wherein the one or more semiconductor fins have a height of approximately 10 nm that is uniform to within 5%.

7. (Currently Amended) The method of claim 1, further comprising: ~~wherein removing any excess semiconductor material from the one or more trenches includes~~ planarizing the semiconductor material to a surface of the trench layer prior to exposing the semiconductor material as one or more semiconductor fins.

8. (Cancelled)

9. (Original) The method of claim 1 wherein filling the one or more trenches with a semiconductor material includes epitaxially growing the semiconductor material within the one or more trenches.

10. (Original) The method of claim 1 wherein filling the one or more trenches with a semiconductor material includes a blanket deposition of semiconductor material.

11. (Currently Amended) An integrated circuit device comprising:

~~a substrate; and~~

~~one or more~~ a plurality of transistors formed upon ~~the~~[[a]] substrate, each transistor of said plurality ~~having~~ further comprising:

an epitaxial semiconductor body~~, each semiconductor body having a height of less than 20 nm, the height of each semiconductor body uniform to within a tolerance of 5% of a specified height~~[[;]]

a gate dielectric on the sidewalls of said semiconductor body, the height of the sidewalls (H_{Si}) being less than 20 nm and uniform within 5% across said plurality of transistors;

a gate electrode on said gate dielectric; and

a source region and a drain region in said epitaxial semiconductor body on opposite sides of said gate electrode.

12. (Currently Amended) The integrated circuit device of claim 11 wherein the ~~one or more~~ plurality of transistors ~~are~~ include tri-gate transistors.

13. (Currently Amended) The integrated circuit device of claim ~~12~~ 11 wherein each semiconductor body has a sidewall height (H_{Si}) of approximately 10 nm.

14. (Currently Amended) A method comprising:

disposing a first oxide layer on a semiconductor substrate;

disposing a nitride layer upon the first oxide layer;

disposing a second oxide layer upon the nitride layer;

selectively etching a portion of the second oxide layer[[,]] ~~and~~ the nitride layer and the first oxide layer ~~to define~~ defining one or more trenches;

filling the one or more trenches with a semiconductor material contacting said semiconductor substrate; and

~~removing the excess semiconductor material from the one or more trenches; and~~

selectively etching a remainder of the second oxide layer ~~and the nitride layer~~ such that one or more semiconductor bodies are formed.

15. (Original) The method of claim 14 wherein the one or more trenches have a depth of approximately 10 nm.

16. (Original) The method of claim 14 wherein the one or more semiconductor bodies have a height of less than 20 nm that is uniform to within 5%.

17. (Original) The method of claim 16 wherein the one or more semiconductor bodies have a height of approximately 10 nm.

18. (Currently Amended) The method of claim 14 ~~wherein~~ further comprising: ~~removing any excess semiconductor material from the one or more trenches includes~~ planarizing the semiconductor material to a surface of the second oxide layer.

19. (Cancelled)

20. (Original) The method of claim 14 wherein filling the one or more trenches with a semiconductor material includes epitaxially growing the semiconductor material within the one or more trenches.

21. (Cancelled)

22. (Original) The method of claim 14 wherein the semiconductor substrate is comprised of a semiconductor material selected from the group consisting of silicon, germanium, and gallium arsenide.

23. (Original) The method of claim 14 wherein the semiconductor substrate is comprised of silicon, the first oxide layer is comprised of SiO_2, the nitride layer is comprised of Si_3N_4, and the second oxide layer is comprised of SiO_2.

24. (New) A method comprising:

forming a first film over a semiconductor substrate;

forming a second film on said first film;

forming a trench in said first film and said second film and exposing the semiconductor substrate;

forming an epitaxial semiconductor film in said trench; and

exposing a sidewall of said semiconductor film by removing said second film selectively from said first film.

25. (New) The method in claim 24, further comprising:

forming a gate dielectric on said sidewall of said semiconductor film;

forming a gate electrode on said gate dielectric; and

forming a source and drain region in said semiconductor film on opposite sides of said gate electrode.

26. (New) The method in claim 24, wherein said first film is a silicon nitride and said second film is a silicon oxide.

27. (New) The method in claim 24, wherein said first film is a silicon oxide and said second film is a silicon nitride.

28. (New) The method in claim 24, further comprising:

removing any excess semiconductor material from said trench prior to exposing a sidewall of said semiconductor film.

29. (New) A circuit device comprising:

a plurality of transistors, wherein the variation in a transistor body height (H_{Si}) across said plurality is less than the variation in a semiconductor body epitaxial film thickness.

30. (New) The circuit device of claim 29, wherein each of said plurality of transistors further comprises:

a semiconductor body having an epitaxial film thickness on a semiconductor substrate,

a gate dielectric on a sidewall of said semiconductor body, wherein said sidewall has a height (H_{Si}) which is less than said epitaxial film thickness;

a gate electrode on said gate dielectric;

a source and drain region in said semiconductor body on opposite sides of said gate electrode.